

Low-Voltage, Low R_{ON} , Dual DPDT Analog Switch

DESCRIPTION

The DG2015 is a dual double-pole/double-throw monolithic CMOS analog switch designed for high performance switching of analog signals. Combining low power, high speed, low on-resistance and small physical size, the DG2015 is ideal for portable and battery powered applications requiring high performance and efficient use of board space.

The DG2015 is built on Vishay Siliconix's low voltage J12 process. An epitaxial layer prevents latchup. Break-before-make is guaranteed.

The switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

FEATURES

- Low Voltage Operation (2.7 V to 3.3 V)
- Low On-Resistance - R_{ON} : 0.85 Ω
- 3 dB Loss at 100 MHz
- Fast Switching: $t_{ON} = 40$ ns
 $t_{OFF} = 35$ ns
- QFN-16 Package
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

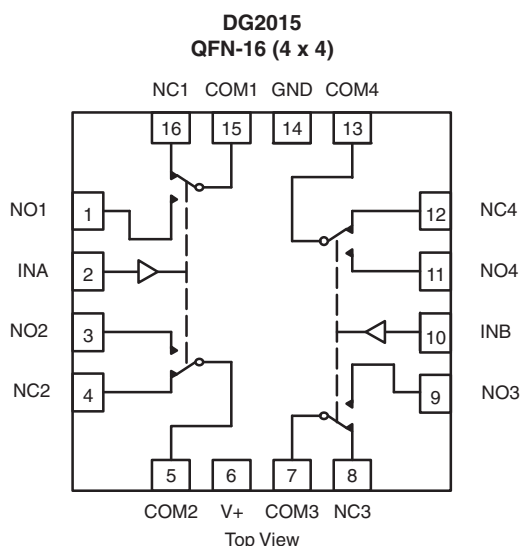
BENEFITS

- Reduced Power Consumption
- High Accuracy
- Reduced Board Space
- Reduce Board Space
- TTL/1.8 V Logic Compatible

APPLICATIONS

- Cellular Phones
- Speaker Headset Switching
- Audio and Video Signal Routing
- PCMCIA Cards
- Battery Operated Systems

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE

Logic	NC1, 2, 3 and 4	NO1, 2, 3 and 4
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION

Temp Range	Package	Part Number
- 40 °C to 85 °C	16-pin QFN (4 mm x 4 mm) (Variation 1)	DG2015DN-T1-E4

ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Parameter	Limit	Unit
Reference V_+ to GND	- 0.3 to + 6	V
IN, COM, NC, NO^a	- 0.3 to ($V_+ + 0.3$)	
Current (Any terminal except NO, NC or COM)	30	mA
Continuous Current (NO, NC, or COM)	± 150	
Peak Current (Pulsed at 1 ms, 10 % duty cycle)	± 200	
Storage Temperature (D Suffix)	- 65 to 150	$^{\circ}\text{C}$
Package Solder Reflow Conditions ^d	16-pin QFN (4 mm x 4 mm)	
Power Dissipation (Packages) ^b	QFN-16 ^c	mW

Notes:

- a. Signals on NC, NO, or COM or IN exceeding V_+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 23.5 mW/ $^{\circ}\text{C}$ above 70 $^{\circ}\text{C}$.
d. Manual soldering with iron is not recommended for leadless components. The QFN is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

SPECIFICATIONS ($V_+ = 3\text{ V}$)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ± 10 %, V _{IN} = 0.4 V or 2 V ^e	Temp. ^a	Limits - 40 °C to 85 °C			Unit
				Min. ^b	Typ. ^c	Max. ^b	
Analog Switch							
Analog Signal Range ^d	V _{NO} , V _{NC} V _{COM}		Full	0		V+	V
On-Resistance	R _{ON}	V+ = 2.7 V, V _{COM} = 0.2 V/1.5 V, I _{NO} , I _{NC} = 100 mA	Room Full		0.85	1.6 1.7	Ω
R _{ON} Flatness	R _{ON} Flatness	V+ = 2.7 V, V _{COM} = 0 V to V+, I _{NO} , I _{NC} = 100 mA	Room		0.16		
R _{ON} Match	ΔR _{ON}		Room		0.15		
Switch Off Leakage Current	I _{NO(off)} I _{NC(off)}	V+ = 3.3 V V _{NO} , V _{NC} = 1 V/3 V, V _{COM} = 3 V/1 V	Room Full	- 1 - 10		1 10	nA
	I _{COM(off)}		Room Full	- 1 - 10		1 10	
Channel-On Leakage Current	I _{COM(on)}	V+ = 3.3 V, V _{NO} , V _{NC} = V _{COM} = 1 V/3 V	Room Full	- 1 - 10		1 10	
Digital Control							
Input High Voltage	V _{INH}		Full	2			V
Input Low Voltage	V _{INL}		Full			0.4	
Input Capacitance	C _{in}		Full		4		pF
Input Current	I _{INL} or I _{INH}	V _{IN} = 0 V or V+	Full	- 1		1	μA
Dynamic Characteristics							
Turn-On Time	t _{ON}	V _{NO} or V _{NC} = 2 V, R _L = 300 Ω, C _L = 35 pF	Room Full		40	65 67	ns
Turn-Off Time	t _{OFF}		Room Full		35	60 62	
Break-Before-Make Time	t _d		Full	1	3		
Charge Injection ^d	Q _{INJ}	C _L = 1 nF, V _{GEN} = 0 V, R _{GEN} = 0 Ω	Room		7		pC
Off-Isolation ^d	OIRR	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz	Room		- 67		dB
Crosstalk ^d	X _{TALK}		Room		- 70		
N _O , N _C Off Capacitance ^d	C _{NO(off)}	V _{IN} = 0 V or V+, f = 1 MHz	Room		63		pF
	C _{NC(off)}		Room		67		
Channel-On Capacitance ^d	C _{NO(on)}		Room		200		
	C _{NC(on)}		Room		196		

SPECIFICATIONS (V+ = 3 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ± 10 %, VIN = 0.4 V or 2 Ve	Temp. ^a	Limits - 40 °C to 85 °C			Unit
				Min. ^b	Typ. ^c	Max. ^b	
Power Supply							
Power Supply Range	V+			2.7		3.3	V
Power Supply Current	I+	VIN = 0 V or V+	Full			1	μA
Power Consumption	PC		Full			3.3	μW

Notes:

a. Room = 25 °C, full = as determined by the operating suffix.

b. Typical values are for design aid only, not guaranteed nor subject to production testing.

c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.

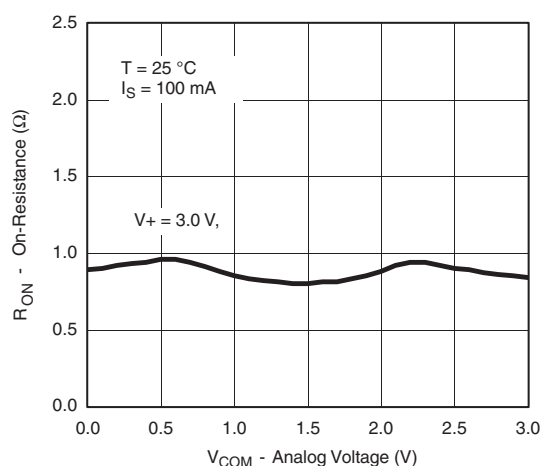
d. Guarantee by design, not subjected to production test.

e. V_{IN} = input voltage to perform proper function.

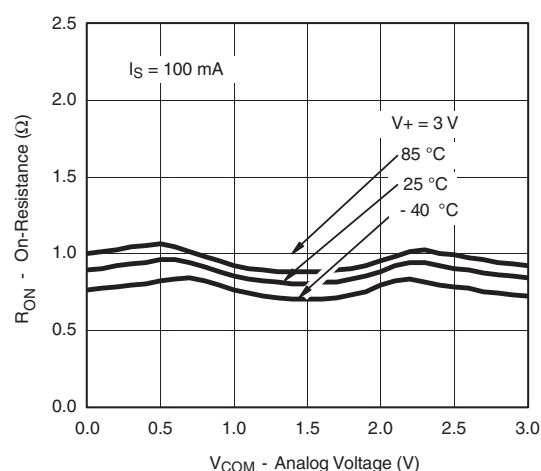
f. Guaranteed by 5 V leakage testing, not production tested.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

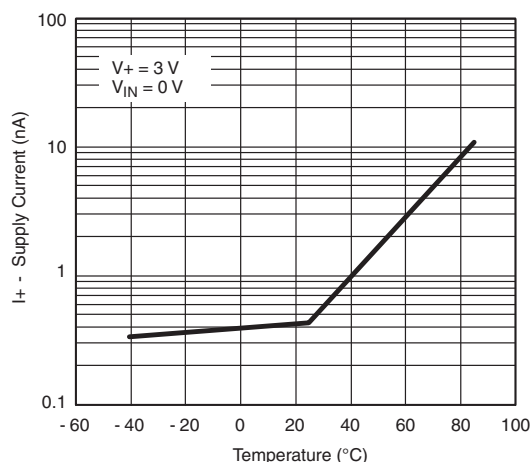
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



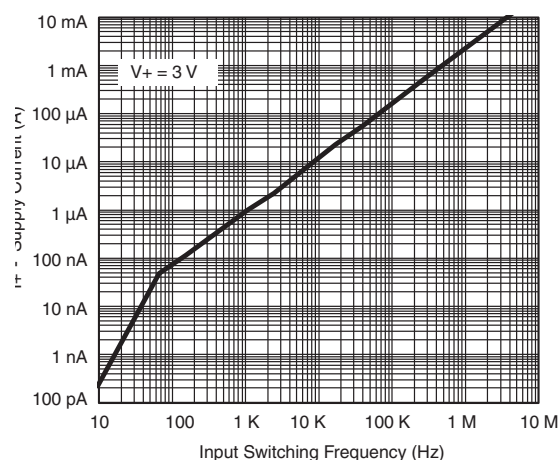
R_{ON} vs. V_{COM} and Supply Voltage



R_{ON} vs. Analog Voltage and Temperature

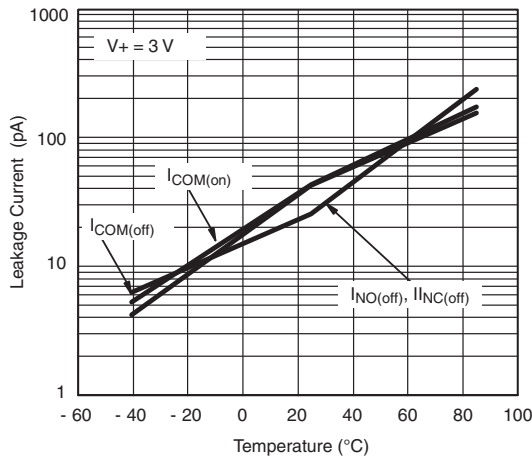


Supply Current vs. Temperature

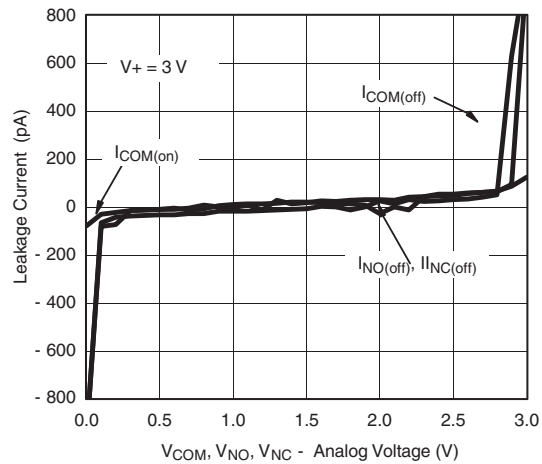


Supply Current vs. Input Switching Frequency

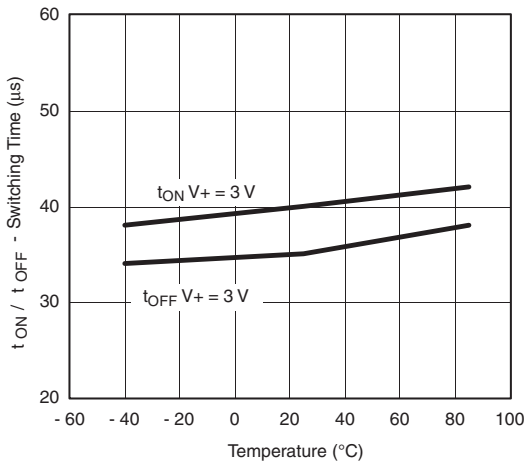
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



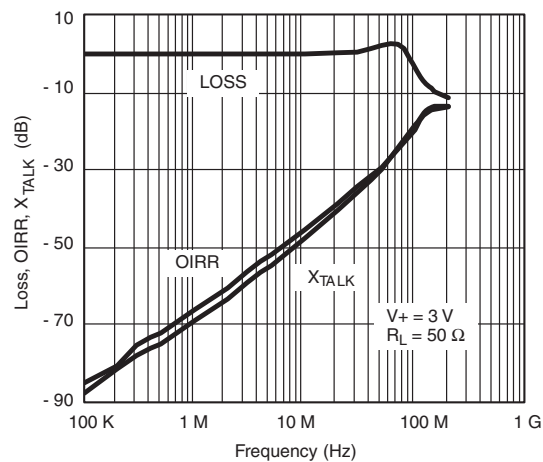
Leakage Current vs. Temperature



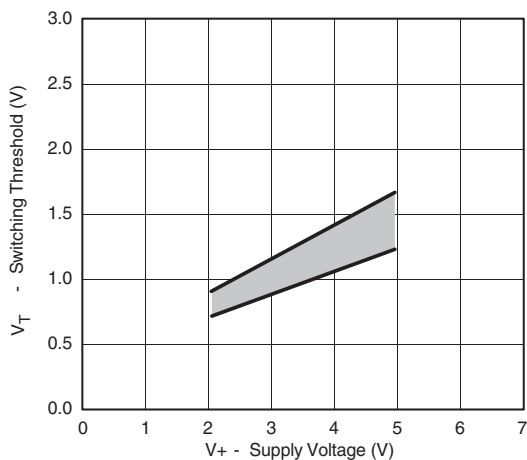
Leakage vs. Analog Voltage



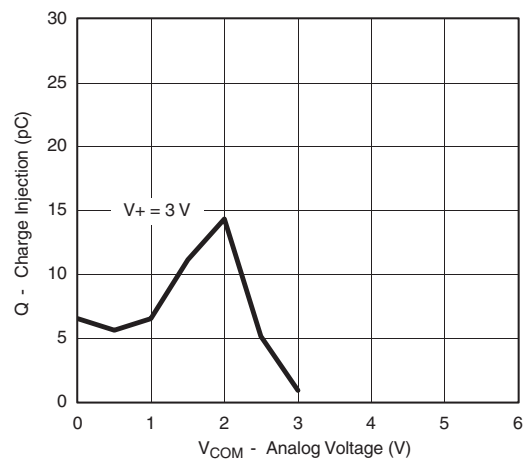
Switching Time vs. Temperature



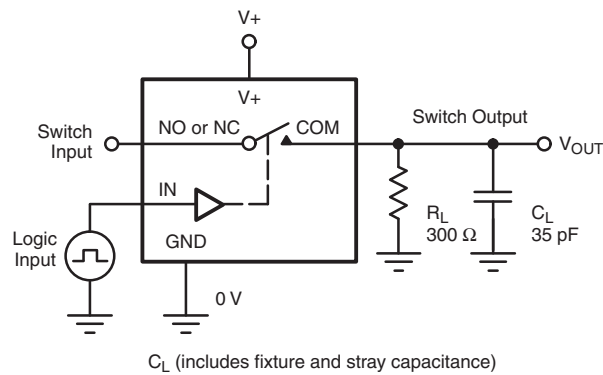
Insertion Loss, Off-Isolation Crosstalk vs. Frequency



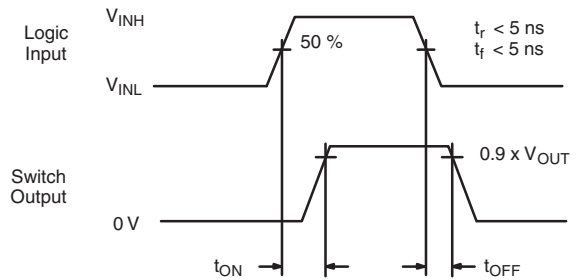
Switching Threshold vs. Supply Voltage



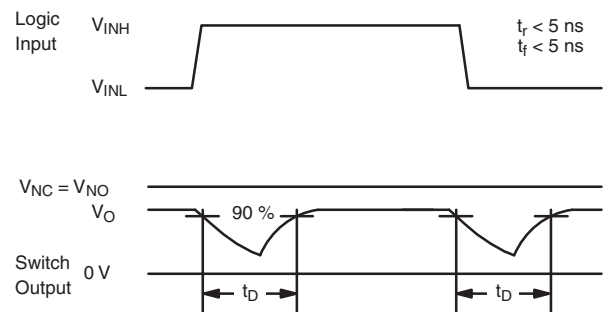
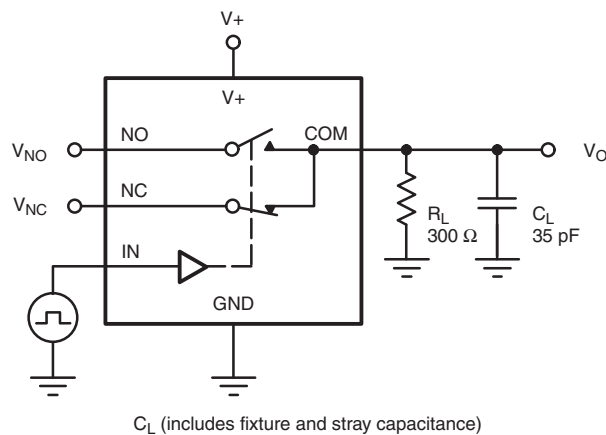
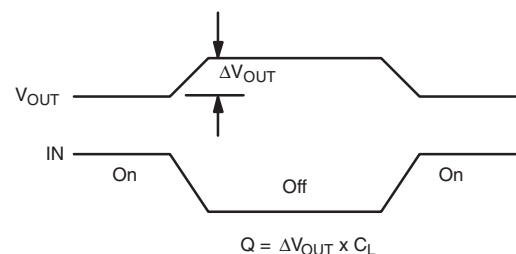
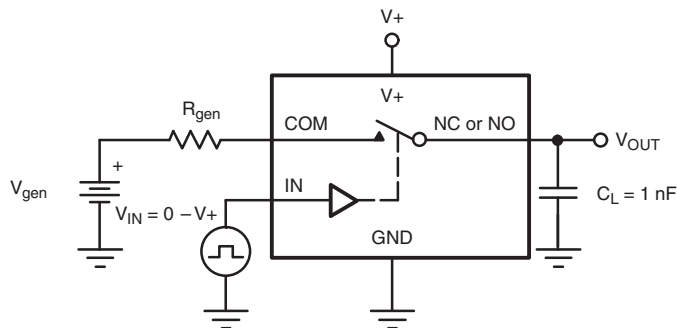
Charge Injection vs. Analog Voltage

TEST CIRCUITS


$$V_{OUT} = V_{COM} \left(\frac{R_L}{R_L + R_{ON}} \right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time

Figure 2. Break-Before-Make Interval


IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

TEST CIRCUITS

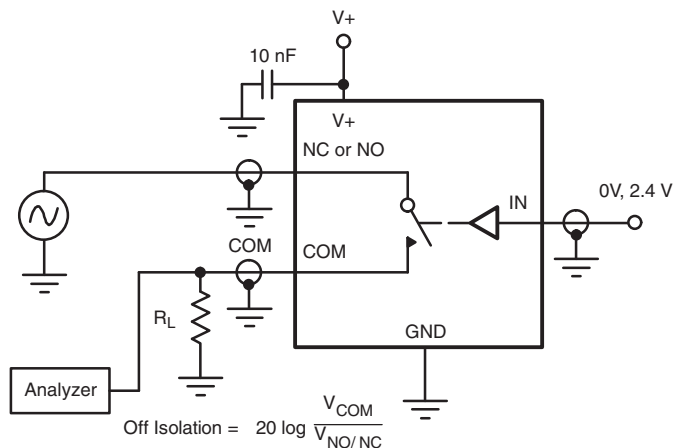


Figure 4. Off-Isolation

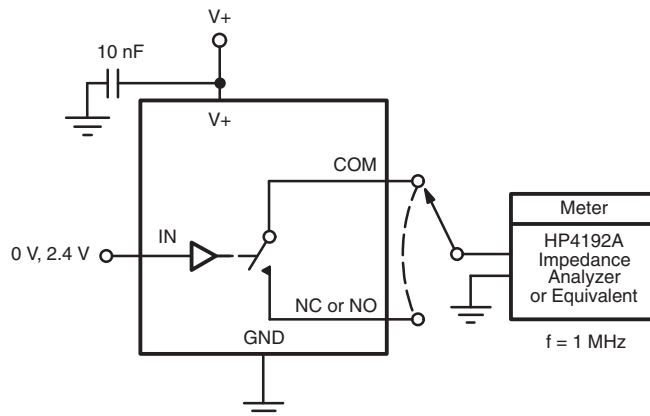
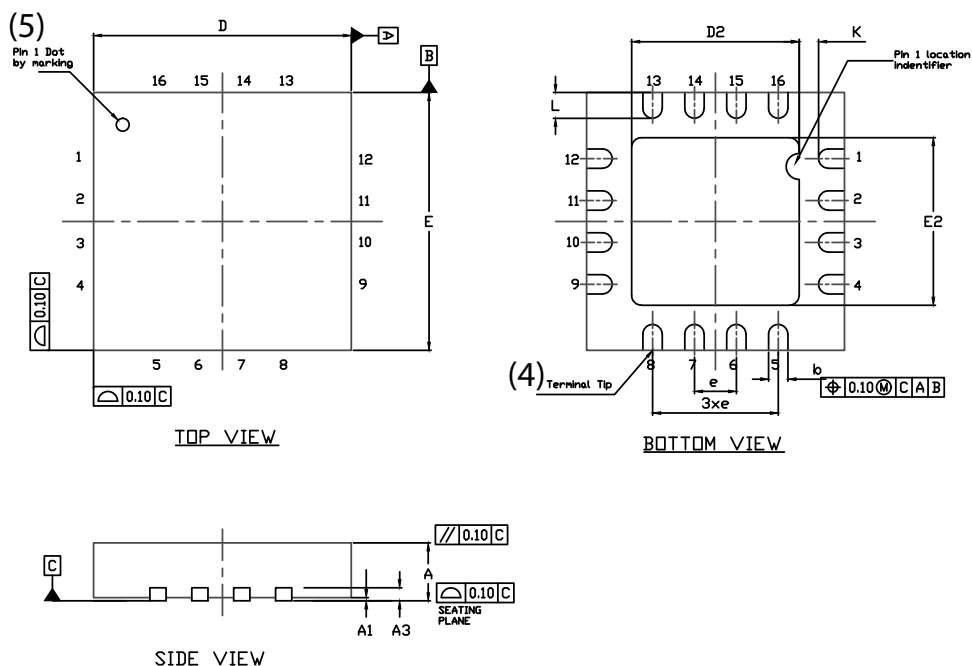


Figure 5. Channel Off/On Capacitance

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71971.

QFN 4x4-16L Case Outline



DIM	VARIATION 1						VARIATION 2					
	MILLIMETERS ⁽¹⁾			INCHES			MILLIMETERS ⁽¹⁾			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.75	0.85	0.95	0.029	0.033	0.037	0.75	0.85	0.95	0.029	0.033	0.037
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
A3	0.20 ref.			0.008 ref.			0.20 ref.			0.008 ref.		
b	0.25	0.30	0.35	0.010	0.012	0.014	0.25	0.30	0.35	0.010	0.012	0.014
D	4.00 BSC			0.157 BSC			4.00 BSC			0.157 BSC		
D2	2.0	2.1	2.2	0.079	0.083	0.087	2.5	2.6	2.7	0.098	0.102	0.106
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
E	4.00 BSC			0.157 BSC			4.00 BSC			0.157 BSC		
E2	2.0	2.1	2.2	0.079	0.083	0.087	2.5	2.6	2.7	0.098	0.102	0.106
K	0.20 min.			0.008 min.			0.20 min.			0.008 min.		
L	0.5	0.6	0.7	0.020	0.024	0.028	0.3	0.4	0.5	0.012	0.016	0.020
N ⁽³⁾	16			16			16			16		
Nd ⁽³⁾	4			4			4			4		
Ne ⁽³⁾	4			4			4			4		

Notes

- (1) Use millimeters as the primary measurement.
- (2) Dimensioning and tolerances conform to ASME Y14.5M. - 1994.
- (3) N is the number of terminals. Nd and Ne is the number of terminals in each D and E site respectively.
- (4) Dimensions b applies to plated terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.
- (5) The pin 1 identifier must be existed on the top surface of the package by using identification mark or other feature of package body.
- (6) Package warpage max. 0.05 mm.

ECN: S13-0893-Rev. B, 22-Apr-13
DWG: 5890



Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay's knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and / or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Hyperlinks included in this datasheet may direct users to third-party websites. These links are provided as a convenience and for informational purposes only. Inclusion of these hyperlinks does not constitute an endorsement or an approval by Vishay of any of the products, services or opinions of the corporation, organization or individual associated with the third-party website. Vishay disclaims any and all liability and bears no responsibility for the accuracy, legality or content of the third-party website or for that of subsequent links.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.